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GATES & COOPER LLP			EXAMINER	
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6701 CENTER DRIVE WEST, SUITE 1050				
LOS ANGELES, CA 90045			ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/582,390	CRAVEN ET AL.
	Examiner	Art Unit Arman Khosraviani 2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If no period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 13 April 2009.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1 and 6-24 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1 and 6-24 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO/0256/06)
 Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____

5) Notice of Informal Patent Application

6) Other: _____

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 4/13/2009 have been fully considered but they are not persuasive. Claim 1 recites the step of "(a) growing one or more non-polar a-plane gallium nitride (GaN) template layers on a substrate, resulting in a grown surface of the non-polar a-plane GaN template layers that is a non-polar plane..." Dwilinski teaches (¶¶ 15-17) growing the GaN template layers on the substrate, which is cut (¶ 109), forming a non-polar a-plane GaN layer, therefore the GaN layer is grown on the substrate to form non-polar a-plane GaN template layers as claimed. Further, Dwilinski teaches (¶¶ 59, 16-17, 27) epitaxially growing gallium nitride containing layers along the non-polar a-plane of the substrate which is cut along a non-polar a-plane surface.

Claim Rejections - 35 USC § 112

2. Claims 21, 22 and 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 22 and 23, do not clearly disclose the structure constituting a c-plane quantum well used for comparison. Additionally, Claim 22 does not clearly state the metric of comparison applied; whether the comparison is the thickness or the maximum emission intensity. Claim 21 does not clearly disclose the structure or plane for polar quantum wells.

Claim Objections

3. Claims 18 and 19 are objected to because of the following informalities: Claims 18 and 19 depend on canceled Claims 2 and 3, respectively. For examination, Claims 18 and 19 are treated as being dependent on Claim 1. Appropriate correction is required.

4. Claims 1, 6-12, 16-20, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dwilinski et al. (WIPO document WO 03/098757)(US 2006/0138431 is used as an English equivalent of WIPO document WO 03/098757)) in view of Hata (US 6,977,953).

Regarding claim 1, Dwilinski teaches (¶¶ 13, 27, 59, 108-111; claim 10) a method for forming a nitride semiconductor device, comprising: (a) growing one or more non-polar a-plane gallium nitride (GaN) template layers on a substrate (¶¶ 15-17, GaN planes: ¶ 109, substrate planes: claim 3), resulting in a grown surface of the non-polar a-plane GaN template layers that is a non-polar plane; and (b) growing one or more non-polar a-plane (Al,In,Ga)N layers directly off of the grown surface of the non-polar a-plane gallium nitride GaN template layers to form at least one non-polar a-plane quantum well. Dwilinski does not teach growing Boron to form the one or more non-polar a-plane (Al,B,In,Ga)N layers off of the grown surface of the GaN layers.

However, Hata teaches (col.9, II.40-45 and col.52, I.43 – col.53, I.4) using boron in a composition of (Al,Ga,In)N to form at least one quantum well.

Since both Hata and Dwilinski teach the method of forming a nitride semiconductor device above, it would have been obvious to include boron for forming the one or more non-polar a-plane (Al_xB_yIn_zGa)N layers off of a grown surface of the GaN layers of Hata in Dwilinski for the benefit of obtaining a desired emission spectra (col.52, l.43 – col.53, l.4).

Regarding claim 6, Hata teaches (col.52, ll.34-42) the substrate is a sapphire substrate.

Regarding claim 7, Dwilinski teaches (¶¶ 81-84) the method above, wherein the growing step (a) comprises: (1) annealing the substrate; (2) depositing a nitride-based nucleation layer (¶ 71) on the substrate (Applicant admits that nucleation layers and uses precursors such as trimethylgallium and ammonia are commonly used in the growth of c-plane nitride semiconductors on ¶¶ 27-28); (3) growing the GaN layer on the nucleation layer; and (4) cooling the GaN under a nitrogen overpressure (¶ 81 wafer is processed in MOCVD device under nitrogen atmosphere from annealing to cooling process) for the same benefit of improving the performance of state-of-the-art optoelectronic and electronic devices by making quantum structures not influenced by polarization-induced electric fields.

Regarding claim 8, Dwilinski teaches (e.g. using MOVCD in Example 1, ¶¶ 92-101) the method above, wherein the growing steps are performed by a method selected from a group comprising metalorganic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), liquid phase epitaxy (LPE), hydride vapor phase epitaxy (HVPE), sublimation, and plasma-enhanced chemical vapor deposition (PECVD) for the same

benefit of improving the performance of state-of-the-art optoelectronic and electronic devices by making quantum structures not influenced by polarization-induced electric fields.

Regarding claim 9, Dwilinski teaches a device manufactured using the method of above (e.g. Example 1, pgs. 6-7, in Example 1 a nitride semiconductor laser device is manufactured ¶ 89) for the same benefit of improving the performance of state-of-the-art optoelectronic and electronic devices by making quantum structures not influenced by polarization-induced electric fields.

Regarding claim 10, Dwilinski teaches (¶¶ 13, 27, 59, 108-111; claim 10) a nitride semiconductor device comprising one or more non-polar a-plane gallium nitride (GaN) template layers on an r-plane substrate (¶¶ 15-17, GaN planes: ¶ 109, substrate planes: claim 3), and one or more non-polar a-plane quantum wells formed from one or more non-polar a-plane (Al,In,Ga)N layers grown off of a grown surface of the non-polar a-plane GaN template layers, wherein the nitride semiconductor device is created using a process comprising: (a) growing one or more non-polar a-plane gallium nitride (GaN) template layers on a substrate (¶¶ 15-17, GaN planes: ¶ 109, substrate planes: claim 3), resulting in a grown surface of the non-polar a-plane GaN template layers that is a non-polar plane; and (b) growing one or more non-polar a-plane (Al,In,Ga)N layers off the grown surface of the non-polar a-plane GaN template layers to form at least one non-polar a-plane quantum well. Dwilinski lacks growing Boron to form the one or more non-polar a-plane (Al,B,In,Ga)N layers off of a grown surface of the GaN layers.

However, Hata teaches (col.9, II.40-45 and col.52, I.43 – col.53, I.4) using boron in a composition of (Al,Ga,In)N to form at least one quantum well.

Since both Hata and Dwilinski teach the method of forming a nitride semiconductor device above, it would have been obvious to include boron for forming the one or more non-polar a-plane (Al,B,In,Ga)N layers off of a grown surface of the GaN layers of Hata in Dwilinski for the benefit of obtaining a desired emission spectra (col.52, I.43 – col.53, I.4).

Regarding claim 11, Dwilinski teaches a nitride semiconductor device, comprising: (a) one or more non-polar a-plane gallium nitride (GaN) template layers on a substrate (¶¶ 15-17, GaN planes: ¶ 109, substrate planes: claim 3), resulting in a grown surface of the non-polar a-plane GaN template layers that is a non-polar plane; and (b) growing one or more non-polar a-plane quantum wells formed from one or more non-polar a-plane (Al,In,Ga)N layers grown off of a grown surface of the non-polar a-plane GaN template layers. Dwilinski lacks growing Boron to form the one or more non-polar a-plane (Al,B,In,Ga)N layers off of a grown surface of the GaN layers.

However, Hata teaches (col.9, II.40-45 and col.52, I.43 – col.53, I.4) using boron in a composition of (Al,Ga,In)N to form at least one quantum well.

Since both Hata and Dwilinski teach the method of forming a nitride semiconductor device above, it would have been obvious to include boron for forming the one or more non-polar a-plane (Al,B,In,Ga)N layers off of a grown surface of the GaN layers of Hata in Dwilinski for the benefit of obtaining a desired emission spectra (col.52, I.43 – col.53, I.4).

Regarding claim 12, Dwilinski teaches (¶ 97) the quantum well ranges in width (40 Angstroms) from approximately 20 Angstroms to approximately 70 Å.

Regarding claim 16, Hata teaches (col.9, II.40-45 and col.52, I.43 – col.53, I.4) the quantum well is a GaN/AlGaN quantum well.

Regarding claim 17, Dwilinski teaches (¶ 97) the non-polar a-plane quantum well ranges in width from more than 40 Å to approximately 70 Å in order to optimize emission intensity from the non-polar a-plane quantum well.

Regarding claims 18-19, Dwilinski teaches (¶ 97) quantum well width of 40 Å, except for the maximum emission intensity from the non-polar a-plane quantum well is associated with a non-polar a-plane quantum well width of approximately 50 Å (or an optimal width of 52 Å). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to have investigated the maximum emission intensity from the non-polar a-plane quantum well to obtain a non-polar a-plane quantum well width of approximately 50 Å (or an optimal width of 52 Å), since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 20, Dwilinski teaches (claim 3) the substrate is an r-plane substrate.

Regarding claim 24, Dwilinski teaches (¶¶ 13, 69) forming the non-polar a-plane quantum well in a manner to maintain material quality and interface roughness, but does not teach an optimal well width of the non-polar a-plane quantum well is determined primarily by material quality, interface roughness, and excitonic Bohr radius.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed the nitride semiconductor device to maintain optimal well width determined primarily by material quality, interface roughness, and excitonic Bohr radius since it was known in the art that these are characteristic properties for determining optimal well width.

5. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dwilinski et al. (WIPO document WO 03/098757) (US 2006/0138431 is used as an English equivalent of WIPO document WO 03/098757)) in view of Hata (US 6,977,953) and in further view of Nagahama et al. (US 6,677,619).

Regarding claim 13, the combination of Dwilinski and Hata fails to teach the quantum well having a doped barrier.

However, Nagahama teaches (col.21, l. 59 – col.22, l. 12) the quantum well having a doped barrier.

Since Nagahama in combination with Hata and Dwilinski teach the method of forming a nitride semiconductor device above, it would have been obvious to have the quantum well with a doped barrier of Nagahama in the combination of Hata and Dwilinski for the benefit of improving power efficiency and lowering the threshold current and voltage of the nitride semiconductor device (col.3, ll.1-11 and col.3, l.60 – col.4, l.16).

Regarding claim 14, Nagahama teaches (col.21, l. 59 – col.22, l. 12) the doped barrier is doped with silicon.

Regarding claim 15, Nagahama (col.21, l. 59 – col.22, l. 12) discloses the claimed invention except for the doped barrier is doped with silicon with a dopant concentration of $2 \times 10^8 \text{ cm}^{-3}$ (Nagahama teaches $8 \times 10^8 \text{ cm}^{-3}$). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to have the doped barrier doped with silicon with a dopant concentration of $2 \times 10^8 \text{ cm}^{-3}$, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Conclusion

THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arman Khosravani whose telephone number is 571-272-6402. The examiner can normally be reached Monday-Friday, 8am - 5pm (Eastern Time).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Arman Khosraviani/

Examiner, Art Unit 2818

8/24/2009

/STEVEN LOKE/

Supervisory Patent Examiner, Art Unit 2818